Detecting Si-Defects with Diodes

Master's Thesis of

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July 12, 1999

Abstract

We explore the use of diode characteristics to detect defects in a silicon wafer.

The characteristics we consider are the turn on and the breakdown voltage, as well as the resistance of the junctions. Also lifetime, low frequency noise and capacity measurements are investigated. The devices we fabricated and tested are regular diodes, pnp-BJT's and MOS-capacitors. The size of the devices is of the order of 100 μm. The silicon defects on our wafer are vacancies (density of vacancy clusters $\sim 1000\,\mathrm{nm}$ is $10^5..10^6\,\mathrm{cm}^{-3}$), which are more in the center of the wafer, and interstitials (density of interstitial clusters $\sim 10^4\mathrm{cm}^{-3}$), distributed on the outer band of the wafer. With vacancies, larger but less abundant defects like Crystral Originated Particles (COP's) also appear.

Eight inch research wafers with a high radial vacancy-to-interstitial gradient were obtained from MEMC Electronic materials. Device arrays were put onto this silicon with collaborators in electrical engineering at University of Illinois. We observed a shift in the I-V curve of pn-junctions of diodes and bipolar junction transistors, one possible explanation for this shift: The radial defect gradient in the silicon.

Contents

List of Figures

List of Tables

1 Introduction

Who's fault is it?

This is a question silicon and device manufacturers pose. Both sides accuse the other of causing the device malfunctions. To clarify, each tests their own work. Hence the silicon manufacturer looks for defects in silicon and the device manufacturer checks the fabrication lines. After all, a device can fail because of a defect in the silicon, or a bad processing step, or even a processing step which causes a defect in the silicon. The reasons for failure are elusive.

Many silicon defects can effect the performance of a microelectronic device. With the rapidly decreasing size of the devices, the influence of small defects increases. While contamination with impurities like metals is brought under control, defects like oxygen precipitates, crystal originated particles (COP's), voids and even structural point defects like self interstitials (I's) and vacancies (V's) play an increasing role.

To find these defects many methods were developed. One of the most direct ones is transmission electron microscopy (TEM), where single atoms can be resolved and silicon defects observed. Defects can be detected non-destructively with confocal infra red microscopy [1]. Other techniques measure the minority carrier lifetime in the silicon. This can be done with photoconductivity measurements, the Elymat technique [2], or surface photo voltaic techniques (SPV) for example.

In this way the relationship between silicon quality and the performance of devices can be studied. Capacitors, and their breakdown are often used to study silicon quality. In this thesis, we explore ways in which non-linear devices (diodes in particular) may be used to study the silicon itself, perhaps improving the symbiotic relationship between silicon and device manufacturers.

2 Existing Methods

2.1 Silicon Defects

One strength of a TEM image is an ability to resolve single atoms, so that defects of any size can be found. This strength is also a weakness, if the density of those defects in the sample is small, i.e. less than $10^8 \mathrm{cm}^{-3}$. In this case, thinning and surveying of enough silicon to find one defect may be difficult. Bigger defects like COP's can be also imaged, as in the work of Deai et al. [3]. Elymat lifetime mapping also prevents wafer reuse, since the silicon surface is treated to hydrofluoric acid. However, minority carrier life time is a very sensitive parameter of the bulk recombination centers. New Elymat techniques detect recombination centers with concentration less than 10^{-3} ppt. To generate the carriers, they have to be excited, e.g. by a Laser. That means that light has to reach the wafer, something not often possible after devices are encapsulated.

To get a prediction of how the wafer will behave when devices are fabricated, the quality of the oxide layer is tested. One way is to process MOS-capacitors on the wafer, and measure C-V characteristics. Breakdown voltage measures the reliability of capacitors, since oxide layers with fewer defects are better insulators. There are even methods to measure the C-V characteristic of a capacitor, without putting a metallic contact on the wafer [4].

2.2 Device Defects

To test devices, the I-V and C-V characteristics can be taken. Faster devices require shorter lifetimes. The life time can be measured for example by observing reverse recovery, as discussed in many textbooks, e.g. [5]. The problem with these methods

is determining the cause of failure.

Another problem in device performance is high noise, which dictates for example the level of thresholds. While the manufacturer tries to keep the noise low, a research field has developed for using noise to characterize devices [6]. Especially the low frequency part of the spectrum is of interest , since the spectrum ends in white noise at high frequencies. The sensitivity is so high, that even single recombination centers can be detected [7]. Noise measurements have the disadvantage of uncertainty about the source of fluctuation measured.

3 Goal of the Project

MEMC, one of the three major silicon manufacturers worldwide, was interested in finding methods to detect silicon defects after devices are put on. Till now, they have used laser confocal IR microscopy and X-ray topography on wafers non-destructively, and cleave and etch or TEM for destructive testing of bulk defects. Gate oxide breakdown of MOS-capacitors is used to measure the quality of silicon oxide. The quality of the silicon may also impact the performance of devices.

The goal of this project is to find new testing methods, telling about quality of the silicon. We begin here to look for probes of silicon defects which are either simple to fabricate or already in place, like pn-junctions or transistors.

4 Theory

This project concerns the effect of silicon defects on devices. We concentrate here on self-interstitials (I's), vacancies (V's) and larger defects formed during the growth of a silicon ingot, like the vacancy clusters referred to as crystal originated particles (COP's). Vacancies and interstitials are point defects. A vacancy is a missing silicon atom at one site, while a self-intersitial is a additional atom between the perfect lattice points. Both defects cause stress in the crystal. If many vacancies accumulate, the possibility of impurity precipitation increases. The most common impurity is oxygen. Vice versa, precipitates attract vacancies to reduce the stress in the lattice generated since precipitated oxygen takes up more room than interstitial oxygen. The size of COP's for comparison, may be few hundred microns.

An oxygen precipitate is an impurity and acts like a trapping or recombination center. Therefore it may be detected by the energy levels it creates in the band gap. Moreover, this defect effects the lifetime of charge carriers. The defects mentioned above are of the same material as the lattice, and are difficult to detect spectroscopically. But they are still defects in the perfect lattice and act as scattering centers. Scattering centers change the mobility of charge carriers.

Big defects like COP's and precipitate clusters, especially when they extend into the insulating oxide layer of capacitors, decrease breakdown voltage. Hence, the parameters effected by these defects include the lifetime, the mobility, and the breakdown voltage of capacitors.

The mobility effects the resistivity and the turn on voltage of a diode:

$$R = \frac{Lt}{w\sigma} \tag{1}$$

with σ =conductivity, L =length, t =thickness, w =width of the diode. Or using the sheet Resistance:

$$R_s = \frac{1}{t\sigma}\sigma = qn\mu \tag{2}$$

with q=charge, n=number of carriers, μ=mobility. Therefore:

$$\mu = (qntR_s)^{-1} \tag{3}$$

If the geometry of the diode is known, the mobility can be directly calculated from equation 1.

From the resistance measurement, the dopant level N can be calculated (see appendix B). With the impurity concentration the turn on voltage V_0 can be derived from:

$$V_0 = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{4}$$

with the intrinsic carrier concentration for silicon n$\approx 1.5 \times 10^{15}\,\mathrm{cm}^{-3}$.

The lifetime τ is the average time a carrier stays in its excited state before recombination. τ decreases with the number of recombination centers. In pn-junctions it is measurable through the storage delay time t_{sd}. t_{sd} is the duration of the current flow in reverse bias after a sudden switch from forward bias. This reverse current then decays with the decrease of the number of carriers. The relation of τ and t_{sd} is described by:

$$t_{sd} = \tau\left[(erf)^{-1}\left(\frac{I_f}{I_f + I_r}\right)\right] \tag{5}$$

with I_f=forward current and I_r=reverse current.

Number and mobility fluctuations of carriers cause noise. The number of carriers is changing with their lifetime, that means with the concentration of recombination centers. Whereas a fluctuation of mobility depends on the number of scattering centers. So, with measuring the power and the shape of the noise spectrum of a pn-junction at low frequencies, silicon defects can be investigated. For mobility fluctuation there is [9]:

$$\frac{S_R}{R} = \frac{\alpha_{meas}}{fN} \tag{6}$$

with S_R=spectral noise power over the resistor R at frequency f with N available carrier.

The Hooge's parameter α_{meas} leads to the mobility:

$$\alpha_{meas} = \frac{\mu_{meas}}{\mu_{lattice}} \alpha_{lattice} \tag{7}$$

where Matthiesen's rule gives:

$$\frac{1}{\mu_{meas}} = \frac{1}{\mu_{impurity}} + \frac{1}{\mu_{lattice}} \tag{8}$$

Since the lattice parameters are listed, the quality of devices can be studied. For devices on silicon α_{meas} is reported to be $10^{-5}..10^{-3}$. The lower α_{meas} the lower the noise, that means the better the device.

The number fluctuation is related to the lifetime of carriers which is called the generation-recombination noise (GR). GR has a Lorentzian spectrum [6]:

$$S_R(f) = \frac{A\tau_{GR}}{1 + (2\pi f \tau_{GR})^2} \tag{9}$$

where A is an amplitude factor depending on the trap density and

$$\frac{1}{\tau_{GR}} = \frac{1}{\tau_c} + \frac{1}{\tau_e} \tag{10}$$

with τ_{GR}=generation recombination lifetime, τ_c=capture time, τ_e=emission time. For higher trap densities this spectrum turns into 1/f-shape.

For single recombination centers, random telegraph noise (RTN) is observed. The spectrum depends also on the capture and emission time τ_{down} and τ_{up}:

$$S(f) = \frac{4(\Delta I)^2}{\left(\tau_{down} + \frac{1}{\tau_{up}}\right)^2 + (2\pi f \tau_{GR})^2} \tag{11}$$

where ΔI is the current amplitude.

The breakdown voltage is found from the C-V measurement of a capacitor. The breakdown occurs when carriers transit the insulating zone which is a SiO_2 layer. Then suddenly the capacitance decreases. The better the silicon oxide is, the higher is the breakdown voltage. Breakdown voltage is not the only parameter giving information about the silicon, but also the shape of the C-V curve. There is:

$$C(V) = \frac{A}{2}\left(\frac{2q\epsilon N_D}{V_0 - V}\right)^{1/2} \tag{12}$$

with ϵ=permitivity, A=area.

5 Present Project

In this project we are looking for device characteristics specific to certain Si defects. There are some silicon defects which don't effect the device performance, whereas others have large effects. We have investigated behaviors of diodes and bipolar junction transistors (BJT's).

Since we know the distribution of defects on our wafer, we are looking for parameters changing in a correlated manner.

5.1 Wafer

The wafer we used was an eight inch in diameter 356 μm thick as grown Silicon wafer from MEMC with no heat treatments. This wafer was p-type with a sheet resistance of 100 Ohm/Area.

We choose this wafer because of the specific defect distribution in it. In the center there are vacancies and towards the edge is a band of interstitials. The center region is 30 to 60 mm, and the outer band is 50 to 80 mm. The density of clusters of these defects is $\sim 10^4 \mathrm{cm}^{-3}$ for the interstitials and $10^5..10^6\,\mathrm{cm}^{-3}$ for the voids (COP's). Dr. Lucio Mulestagno from MEMC confirmed.

5.2 Devices

Dane Sievers from the University of Illinois helped us to process the devices on the MEMC wafer. We used the microelectronics fabrication lab at the University of Illinois in Urbana-Champaign which includes a t1000 cleanroom. This lab is made for undergraduate microelectronics lab courses [8].

To have the possibility to investigate many different kinds of devices and their

parameters, we processed on the wafer the standard device set for this ece344 class. This consists of 24 cells with many different devices including diodes, bipolar junction transistors (BJT's), field effect transistors (FET's), metal-oxide-silicon(MOS)-capacitors, resistors and oscillators. A cell is 8 mm long and 6 mm wide. So the devices are of the order of a couple of hundred microns. Figures of the mask and the device cell are in figure 1 and figure 2. The wafer and the device design is in figure 9. The major processing steps are listed in appendix A.

5.3 I-V Characteristics

We measured the I-V characteristic of pn-junctions to examine the mobility of carriers in the silicon. We investigate the pn-junctions in both, diodes and BJT's. The forward bias current gives the turn on voltage, and the slope of the current leads to the resistivity of the diode. The way these reflect mobility is derived in section 4.

5.4 Apparatus

We measured the base-emitter (BE) and the base-collector (BC) junction of the BJT's in Dane Sievers lab with a HP-curve tracer. The devices were contacted via a probe station, and data received through the IC-CAP software. The forward bias was 0..5 V and the current was 0..60 μA. The reverse bias was 0..15 V at currents 0..2.5 mA.

At UMSL we used a Tektronix 571 curve tracer to plot I-V characteristics, and measured the I_{CE} vs. V_{CE} to receive the amplification factor β. The forward bias was 0..5 V and the reverse bias up to 100 V. The maximal power P_{max} through the devices was 0.1 Watt and the resitance loaded R_{load} on the device was 10 Ohm.

The diodes were tested at UMSL with the same set up as for the BJT's. The forward bias was 0..1 V the reverse bias 0..10 V; here $P_{max} = 0.5$ Watt and $R_{load} =$ 10 Ohm.

5.5 Desired Results

The turn on voltage is a function of the dopant concentration as shown in equation 4. So, if the defects attract carriers, the V_0 should change with the distribution of the defects, i.e., radially. Or, if just the big defects like COP's, voids and oxygen precipitate clusters attract carriers, V_0 should be constant all over the wafer, with some peaks at devices close to those defects.

From equation 1 we know that the slope of the I-V curve is given by the resistivity R of the silicon. For $R \sim \frac{1}{\mu}$ the effect of the mobility will be represented by the change of R. Since every deviation from the perfect lattice decreases the mobility, not just the local big defects should be noticeable, but also the gradual change of the I and V density should give a gradual change of R.

5.6 Results: BJT's

Vertical BJT's are investigated. We choose the recommended transistors, which are the first and the third BJT in the lower row from left (see figure 3) from the same cell. V_0 of the BJT junctions are between 200 and 400 mV for the BC-junction and 5 and 7 V for the BE-junction. The reverse bias breakdown occurs for the BE-junction 2 to 7 V, whereas the BC-junction broke down between 5 and 13 V (see the table 1). This range is confirmed by the testing at UMSL, where the BE-junction turned on between 2 and 5 V and broke down between 4 and 18 V. But this time we observed also breakdown voltages up to 90 V. The BC-junction behaves similarly

to the previous measurement, that means V_0 between 280 and 450 mV, and V_{break} varying from 2 to 6 V. This results are to find in table 2.

In our case not just the values are important but also the relation to the position on the wafer. Therefore, we mapped the results in figure 3. We observed also very low saturation currents around 5 to 10 μA. β between 100 and 200 is observed. We haven't measured the resistance.

5.7 Conclusion: BJT's

We expected to see a pattern in the varying of the voltages, but no correlation is found. We noticed low V_0 values. If calculated with the sheet resistance of the wafer, V_0 should be around 0.7 V. That means the measured values are lower than calculated by a factor of 2. Still, it is not surprising for these kind of flat devices. Similar to V_0, V_{break} is also lower than for regular diodes, which have $V_{break} > 100$ V. V_0 of the BC-junction is so high that it seems to be more a secondary breakdown, rather than a turn on voltage. With these data, there cannot be a relation to the defects found, since no pattern for the distribution appeared.

The I-V characteristic leads to the conclusion that the pn-junctions of the BJT's are not performing well. This can be due to the fabrication process. On the other hand, amplification factors of β=100..200 show that some the transistors are amplifying.

5.8 Results: Diodes

The square and round diodes (see figure 4) were also tested. In analogy to the BJT junctions, V_0 is between 350 and 550 mV and V_{break} between 2.6 and 7.7 V, comparison to table 3. We see a pattern when mapping the values (see figure 8).

Both voltages for both diode shapes are decreasing from the corner 4 to the middle of the side A.

The evaluation of the resistivity leads to values between 600 and 2200 Ohm (compare table 3). No pattern can be found relating these values for the resistance to the defect distribution. Compare map in figure 7.

5.9 Conclusion: Diodes

Similar values for BJT's and diodes show the reliability of the voltage measurements. To relate the pattern of voltages to the defect distribution, the fabrication process has to be recalled. The wafer was sitting with side C on the boat, in the furnace during the predeposition and diffusion process. Therefore symmetry to an axis (called z-axis) perpendicular to this side can be assumed. Further, gravitation and turbulence could cause a gradient of the dopant concentration in the z direction. With this assumption and no other influences, the devices in the cells of the same row (perpendicular to z called x, i.e. the same distance from side C) should have the same doping due to diffusion and therefore show the same performance.

But V_0 and V_{break} vary noticeably in the x direction as listed in table 4. This gradient in the x direction leads to the conclusion that there is an influence in that direction. The only parameter having a x-component is the radial distribution of the silicon defects. So, I's and V's may modify accumulation of donors and acceptors, recalling equation 4, since they themselves have no electrical effect.

The fact that there is no such pattern observed in the resistivity measurement, no evidence for a mobility dependence can be reported. That does not necessarily mean that there is not such an effect, but just that we can not detect one. We also observed a relation between resistivity, saturation current, and the corrosion of the

devices. With decreasing quality of the contacts, the resistivity increases and the saturation current decreases.

5.10 Improvement

The fabrication process is the most limiting factor to accurate measurements. Therefore it is recommended for future projects that we pay more attention to fabrication quality. Measurements of the sheet resistance at each step will improve the accuracy, and clear up speculation about the dopant uniformity.

Also, focusing on just one kind of device will improve the accuracy, since more devices of the same kind can be tested and there are no other parameters to cause performance changes, like unneeded lithographic steps.

All this might be achieved it we have access to a local fabrication facility.

6 Lifetime

As earlier introduced in section 4, we can use reverse recovery to measure lifetime of the carriers.

6.1 Apparatus

We use a signal generator to bias the diode with square waves. The rise time is 20 ns. To detect the storage delay time, we use a digital 100 MHz oscilloscope. With this scope we are able to detect signals of the order 10 ns.

6.2 Desired Results

Defects effecting the lifetime are traps and recombination centers. Since COP's, voids I's and V's have the same atomic structure as the lattice, they are not supposed to influence the lifetime. But if they for example attract other impurities, the lifetime should change with the defect distribution. A regular diode has a storage delay time t_{sd} of the order of milliseconds.

6.3 Results

With our equipment we are not able to see a storage delay time. But our test of regular diodes worked. So there is no problem with the set up. On the device diodes, we observe a rounding of sharp edges of the input signal in the output.

6.4 Conclusion

We may not have seen a t_{sd} because of the size of the devices. In such a small area of the depletion zone there are not many carriers, keeping up the current. So, the reverse current saturates very quickly. The rounding of the input signal shows capacitance effects, mainly from the wires connecting the probes with the scope.

It can not necessarily be assumed that the defects we are investigating are causing the short storage time, since no characteristic relation to the defect distribution is observed.

6.5 Improvement

For future investigations, faster signal generators and detectors might help. Increase of the time resolution by one order of magnitude should lead to results. However, for such high frequencies, also different probe wires, e.g. coaxial, will also be necessary.

7 Noise

The advantage of noise measurements is that they allow to test mobility μ as well as lifetime τ. If independent measurements regarding μ or τ have been done, noise measurement can be very instructive.

7.1 Apparatus

There are two main challenges to a noise measurement. The first one is shielding from external noise, the second is the amplification from the small noise signal of the device under testing (DUT).

The sample as well as the preamplifier have to be shielded. If a low noise operational amplifier is used, a small box covering the wafer and the op-amp with holes for the probe tips is sufficient. If a complete preamplifier is used, the whole probe station has to be covered. In the first case a massive box has to be build of good conducting material to keep out the electrical part of the radiation. For the magnetic part a layer of μ-metal or soft iron is recommended. Good conduction materials are Ag, Cu or Al. For the second case, a shield with a conductive mesh is preferable because of convenience. The material requirements are same as above.

The low noise amplifier should be powered by batteries. Since batteries have naturally low noise. This is necessary to keep the DUT noise from being swamped.

The signal fluctuations in voltage across the DUT is best coupled capacitively with the amplifier for higher frequencies. For very low frequencies, the coupling capacitor should be bypassed. The parameters of this measurement are applied voltage, and the resulting current through the DUT.

7.2 Desired Results

If applied in addition to other tests, noise measurement is a very useful tool for finding defects, even at low densities. Moreover, slightly different behaviors of mobility, and carrier number fluctuations, might help even to distinguish defects.

The higher the scattering center density (I's and V's), the higher is the μ related noise. For high trap and recombination center densities (hence abundant impurities causing such centers), the fluctuations in carrier numbers should be dominant.

8 Capacitors

The breakdown voltage of capacitors is a measure of the quality of the silicon oxide. We used this method to compare our data with MEMC's results. Also, the C-V curve of pn-junctions is investigated, to get information about the dopant level.

8.1 Apparatus

To measure the breakdown voltage of MOS-capacitors we used an HP LCR meter. The LCR meter from St. Louis University determines the capacity of the DUT for several bias voltages. We also used a C-V plotter from UMSL to get these results. The C-V curves of the pn-junctions were earlier taken at the University of Illinois with a HP curve tracer and IC-CAP software.

8.2 Desired Results

Since I's and V's are point defects they are not supposed to effect the breakdown voltage, but bigger defects like voids do. Therefore the breakdown voltage should relate to density of voids. As mentioned earlier, however, void like defects (COP's) are not independent of the point defects. Hence, lower breakdown voltages should appear in regions of high COP density, i.e. in the V rich zone near the center of the wafer.

From the C-V curves we hope to confirm the turn on voltage V_0 of the diodes, like derived in equation 12, so that the reliability of these measurements is proved.

8.3 Results

Our data show very low, and extremely unstable, capacitances. We assume the reason are the wires and the set up. Therefore no data were recorded.

We were not able to get the 1/V behavior of the characteristic, as derived in equation 12. Moreover, the capacity breaks down at a certain voltage, ending up at a negative value. This breakdown could not be correlated to the reverse bias breakdown.

8.4 Improvements

Instead of the sophisticated HP LCR meter we borrowed from St. Louis University for these measurements, a simple C-V plotter will lead to the same results. Also the set up has to be improved, so that the capacitance of the probes and there connecting wires don't effect the measurement. As follow-up, we may ask MEMC to repeat these tests in their breakdown testing facility.

9 Summary

We observed a shift in the turn on voltage of pn-junctions which might be due to interstitials and vacancies in silicon, because the pattern of the shift in part correlated with the distribution of these defects. It is possible, therefore, that vacancies facilitate dopant diffusion. If so, this effect would not occur on devices doped by implantation. No effect of I and V defects on the mobility of carriers was detected.

We also explored reverse recovery, capacity and noise measurements as test methods to obtain device parameters which reflect the quality of the silicon wafer.

In this case, the fabrication of the devices was a severe limiting factor. Local fabrication facilities and/or collaboration with device manufacturers, is therefore recommended for future work.

10 Outlook

One of the corollary goals of this research work, perhaps the most important goal, was the assembly of device-related resources in this region to open new doors for further projects. Till now, for the semiconductor industry the University of Missouri - St. Louis has been primarily a center for microscopy. By pooling regional resources from MEMC, St. Louis University, Washington University, and University of Illinois, we have now begun research on semiconductor devices. With some effort, it may even be possible to build up a fabrication lab in this area. We thus report here first time work with:

- a fabrication lab at the University of Illinois - Urbana via Dane Sievers
- a probe station in Daniel Leopold's lab
- a tektronics 571 curve tracer for device testing in Roobik Gharabagi's lab
- a HP LCR meter is in Bernard Feldman's lab as well as in Gharabagi's
- a low noise preamplifier and a low frequency spectrum analyzer are to be found in Peter Handel's lab
- also some fabrication equipment is located in Leopold's and Gharabagi's labs

The human resources are:

- Dr. Lucio Mulestagno - a semiconductor and microscopy expert from MEMC
- Dr. Phil Fraundorf - expert on microscopy and semiconductors from UMSL
- Dr. Roobik Gharabagi - expert on semiconductor devices, Electrical Engineering SLU

- Dr. Daniel Leopold - expert on semiconductor devices, Wash U/ UMSL
- Dr. Peter Handel - expert on noise measurements, UMSL
- Mr. Dane Sievers - expert in microelectronics processing, U of I - Urbana

If these forces continue to work together, this area could become as well known for work on microelectronic devices device as it is for its research on semiconductors.

11 Acknowledgement

I would like to acknowledge all the people supporting this project. First I mention my advisor, Phil Fraundorf, who helped me to organize and finally realize this project. Then there is Lucio Mulestagno, who provided the wafer, and Dane Sievers, who spent his time going through the fabrication process with us. I also want to emphasize the generous offer of Daniel Leopold and Peter Handel, for use of their equipment. I like to acknowledge Wayne Garver's advice in matters electronic. I also want to thank my graduate advisor, Bruce Wilking, for helping me to find my way in this year as graduate at UMSL.

Finally, there are two people I want to thank most. It is still difficult for me to believe how much time and effort Roobik Gharabagi spent with me working on this project. We went together through all the steps, beginning with the search for literature ranging from the fabrication process, up to the testing, analysis, and writing of this report. He always found time for me, no matter if it was 8 a.m. in the morning or 10 p.m. at night in his house. Thank you so much Roobik.

The other person is my brother, Dominik. I don't think I would having survived the last days without his support. Thanks bracho.

12 References

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13 Tables

BJT Characteristics

Cell	1. BJT	BC	1. BJT	BE	3. BJT	BC	3. BJT	BE
	FB[mV]	RB [V]	FB	BR	FB	RB	FB	RB
2	292	4.80			7.01	12.01		
6	205	6.15	330	6.34	6.55	11.96	5.55	11.90
10	294	6.20		6.35	6.12	11.64	6.14	11.63
12	585	2.92	290	2.93	6.28	14.07	7.16	13.95
13	250	5.85	292	6.05	6.8	11.70	6.88	11.73
15	249	2.55	245	2.93	6.84	10.95	6.92	10.25
17	248	5.23	425	5.30	6.04	12.05	4.72	5.25
19	300	2.29	258	2.48	6.78	14.70	6.20	13.95
22	343	7.02	326	7.05	5.31	11.25	5.10	11.16
23	278	4.25	287	4.35	6.42	12.70	6.64	12.40

Table 1: BJT pn-junctions, U of I

BJT - UMSL measurement

BJT's cell no.	β	BE FB [mV]	BE RB [V]	BC FB [mV]	BC RB [V]
6.1	111	3730	90	450	6.37
9.1	137	5000	88.2	340	5.28
16.1	127	255	4.06	283	4.55
19.1	212	1980	18.11	330	2.26

Table 2: BJT pn-junctions, UMSL

Diode Characteristics

Cell Number	square diode FB [mV]	RB [V]	R [Ohm]	round diode FB [mV]	RB [V]	R [Ohm]
1	420	4.29	1085	425	4.34	8.49
2	393	5.19	920	407	5.14	731
3	332	3.36	950	322	3.40	873
4	346	4.53	1297	336	4.58	1439
5	382	5.56	1368	377	5.66	1274
6	416	6.31	1392	416	6.36	1274
7	318	3.43	1344	308	3.53	1274
8	336	4.51	1462	341	4.53	1415
9	425	5.51	849	416	5.61	849
10	420	6.75	1792	420	6.70	1557
11	368	2.40	755	359	2.64	1580
12	290	3.67	1627	290	3.67	1722
13	383	6.54	1014	383	6.68	967
14	462	4.81	1040	443	7.74	1863
15	368	3.44	1604	368	3.54	1533
16	364	4.63	1014	369	4.67	1014
17	547	5.89	2193	430	6.03	2123
18	542	7.20	1226	542	7.20	896
19	369	3.46	1108	374	3.60	1038
20	424	4.91	1627	420	5.00	1604
21	514	6.26	1015	523	6.21	802
22	477	7.71	1015	481	7.76	731
23	533	5.14	635	533	5.42	613
24	481	6.89	710	481	6.98	708

Table 3: Diode characteristics

Voltage variation

Row from	3	4	5	6
to	19	20	21	22
ΔV_0 [mV]	52/37	84/78	146/132	65/61
ΔV_{break} [V]	0.2/0.1	0.42/0.38	0.55/0.73	1.40/1.40

Table 4: Difference due to Si-defects

14 Figures

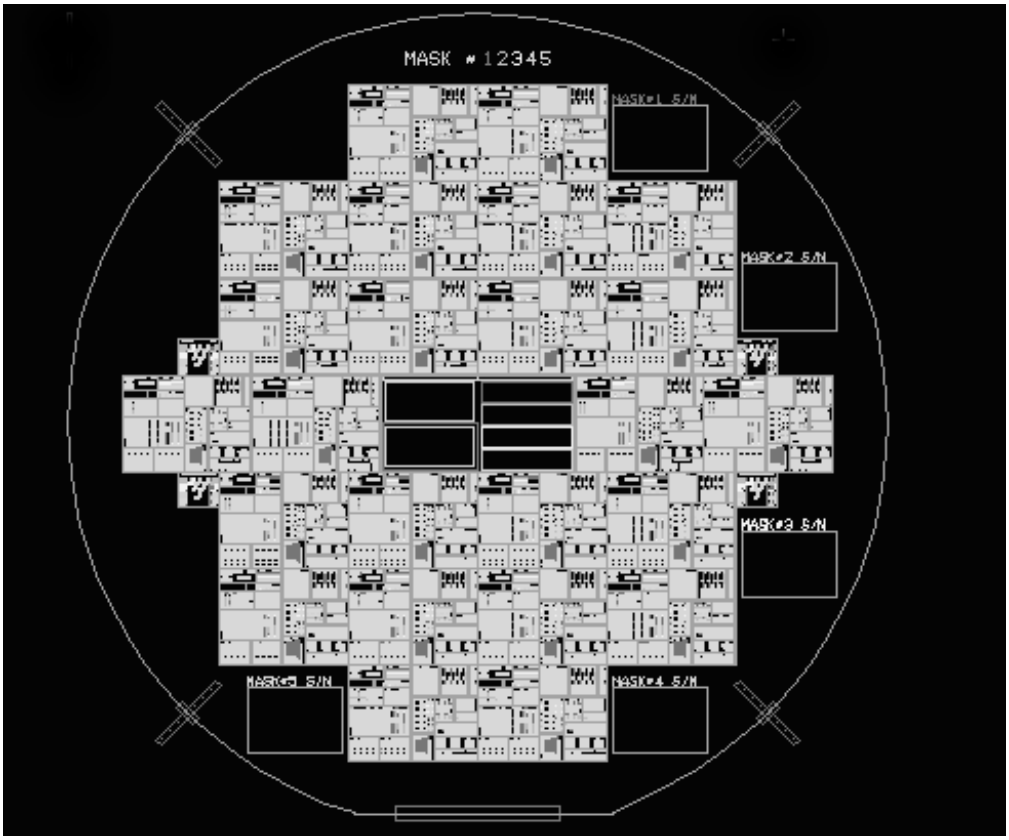

Figure 1: Mask for device set

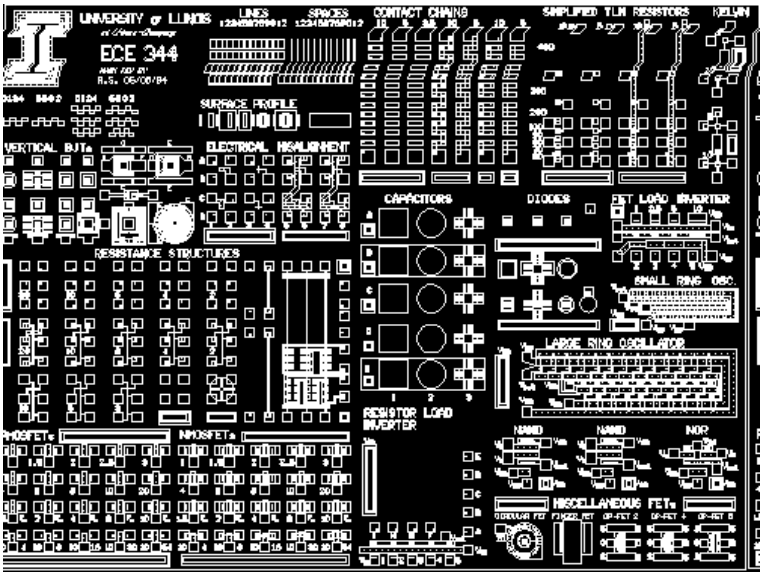

Figure 2: Device cell

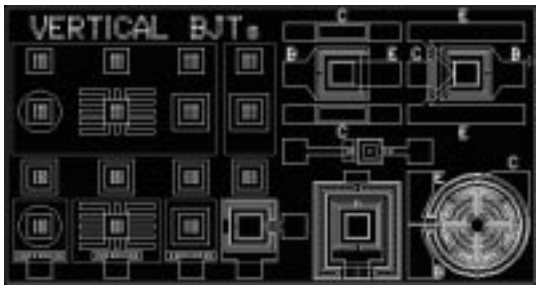

Figure 3: Vertical BJT's

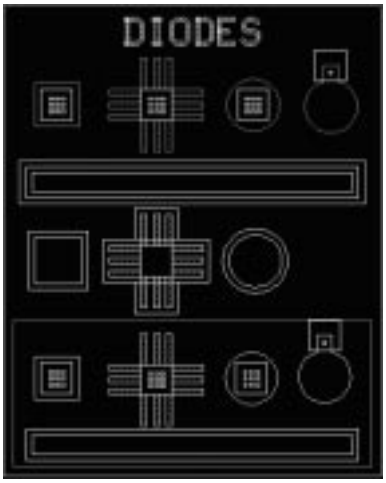

Figure 4: Square and round diodes

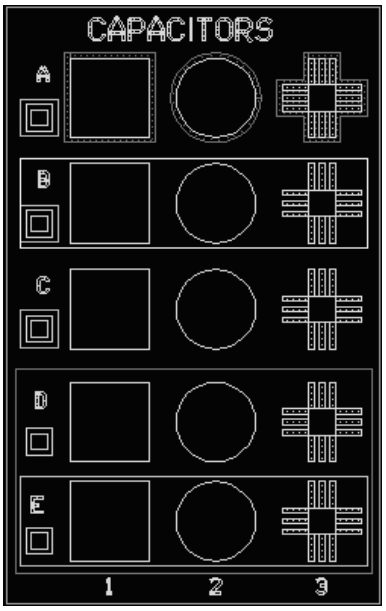

Figure 5: MOS-capacitors

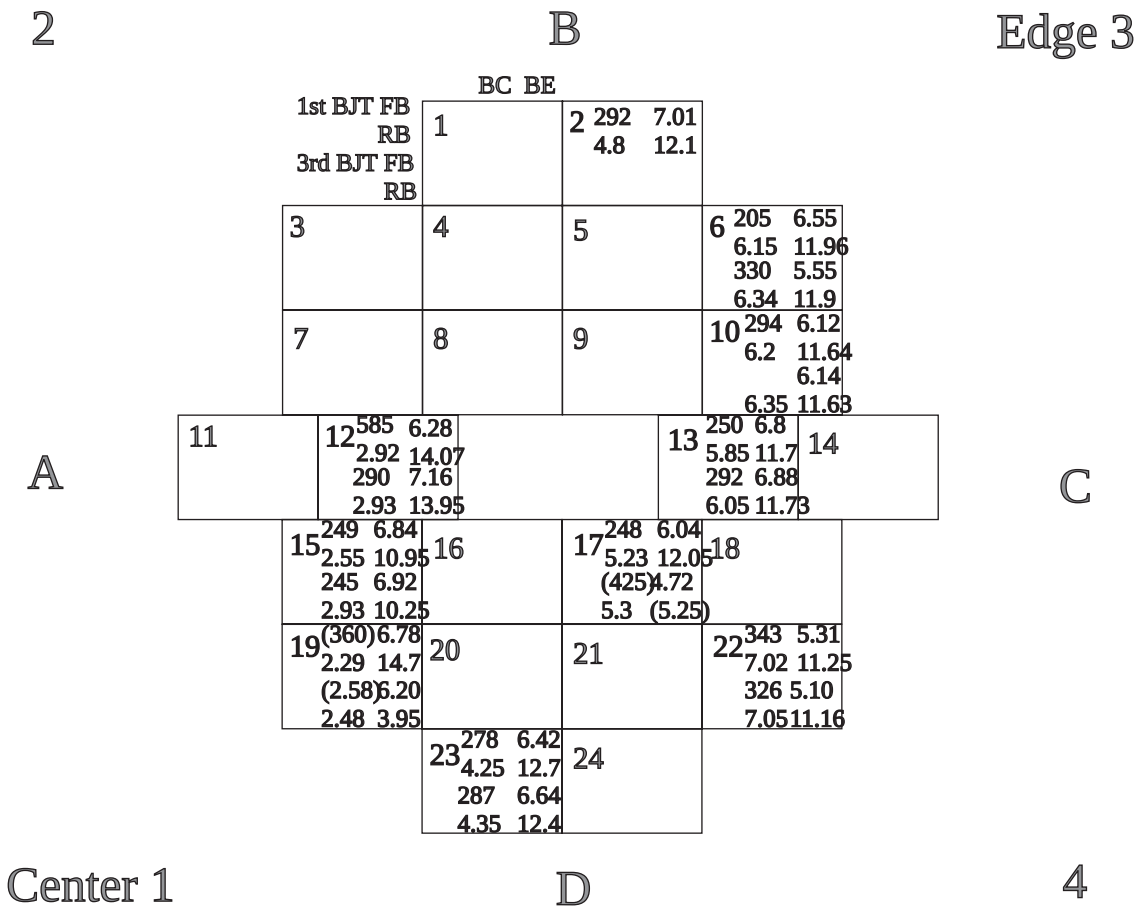

Figure 6: Mapped BJT characteristics

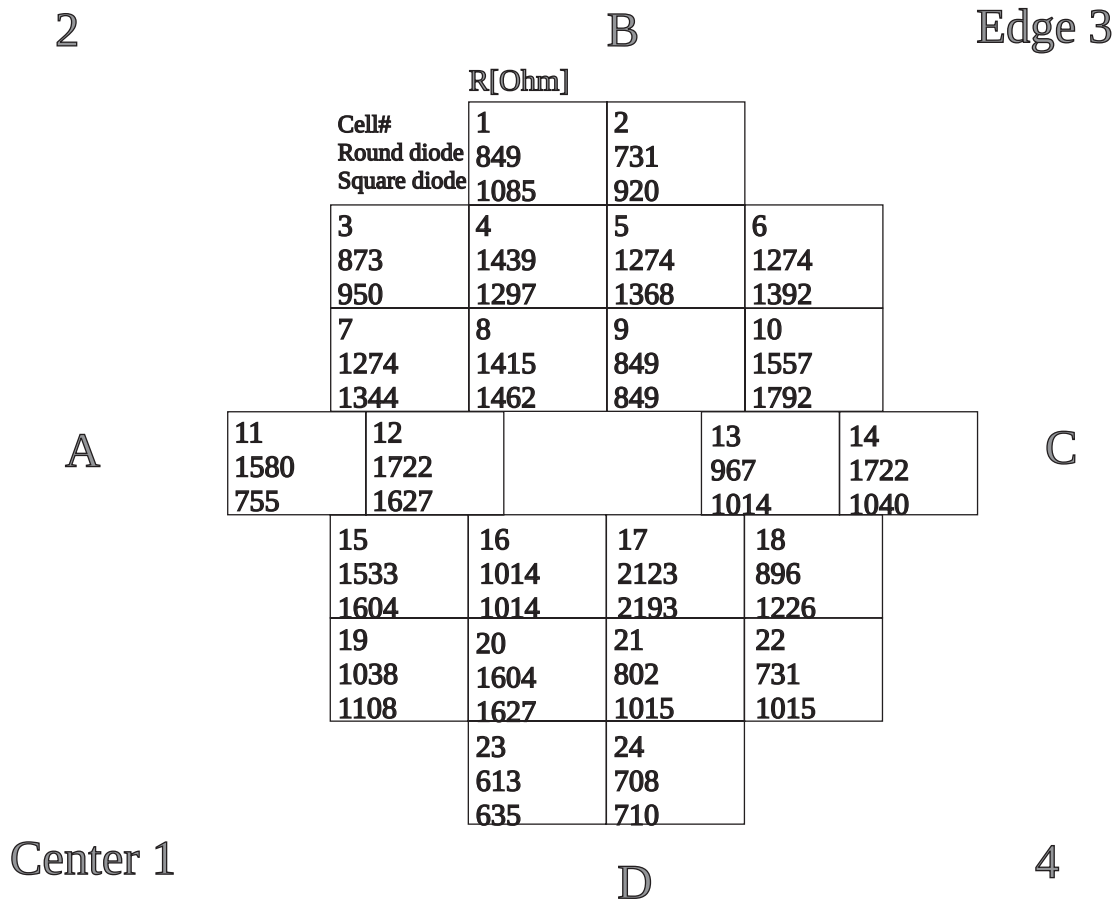

Figure 7: Mapped diode resistivity

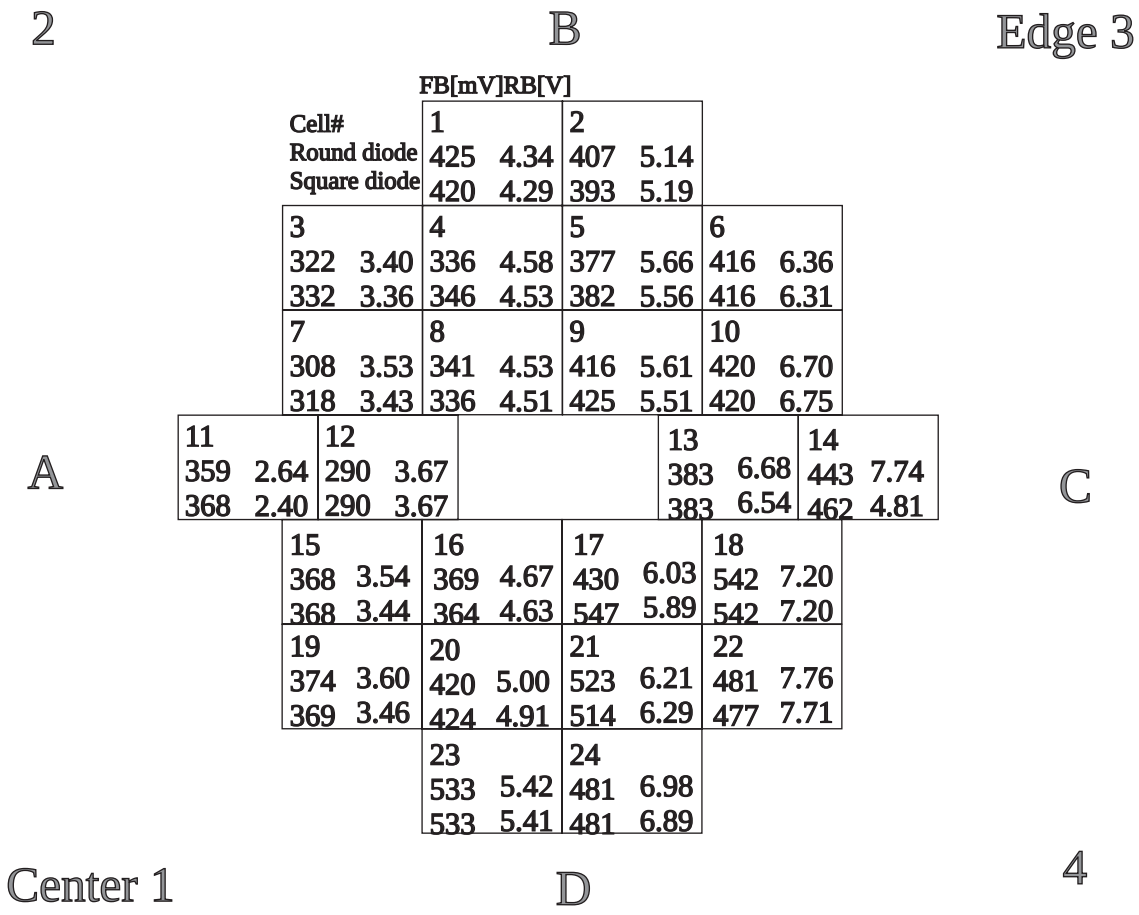

Figure 8: Mapped diode characteristics

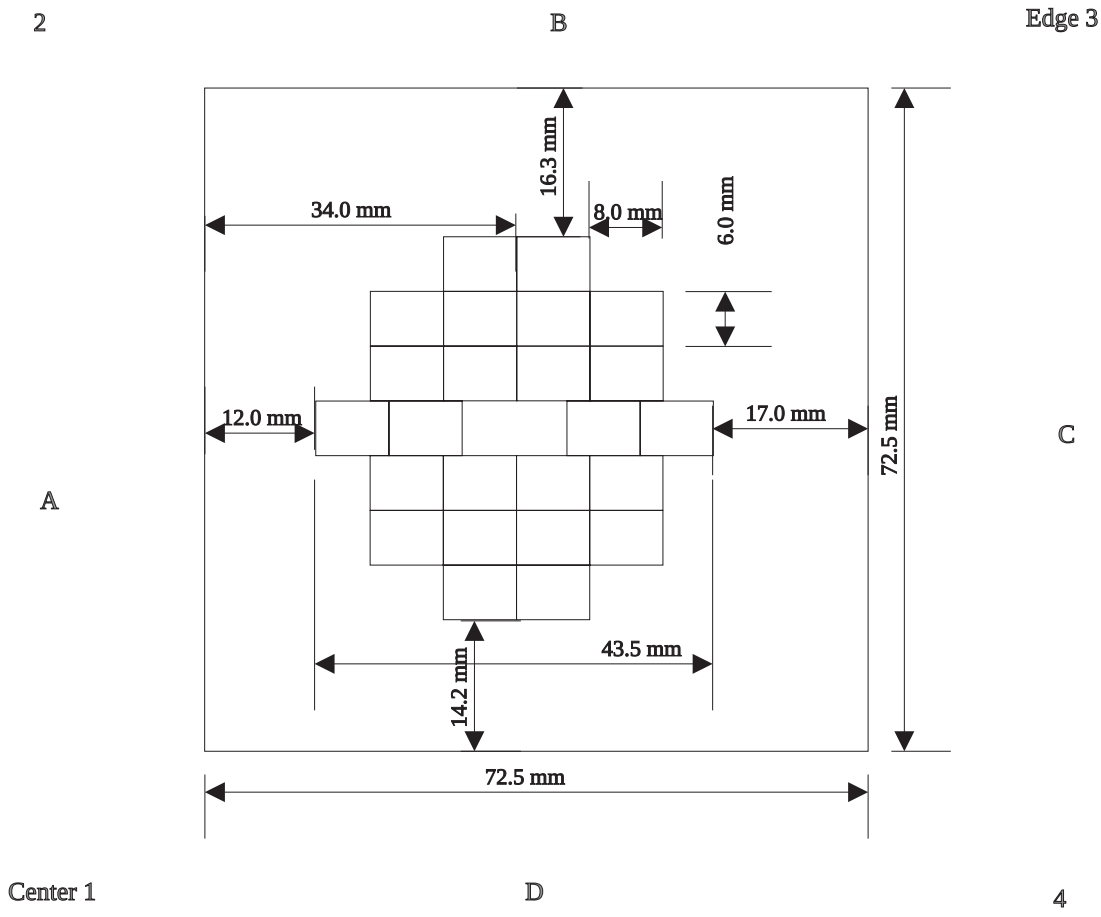

Figure 9: Device design - position on the wafer

A Processing

First, we note that the facilities in Dane Sievers lab can not handle eight inch wafers. Hence, the MEMC wafer had to be cut into four pieces. We ended up with four squares about 72 mm on a side, with one rounded corner (cf. the design in figure 9). Crucial steps:

1. RCA clean
2. initial oxidation at 1100°C to grow a 1500Å thick silicon dioxide layer
3. spin on positive photo resist (PR)
4. bake PR and align the mask
5. expose PR and remove it with the oxide layer
6. 10 min. Phosphate predepostion at 1000°C
7. 40 min. drive to diffuse P deeper in the Si and growing an 2900Å oxide layer
8. next PR step
9. 15 min. Born predeposition at 950°C
10. 30 min. drive
11. further PR steps and contact annealing

B Diode Characteristics

A diode is basically a pn-junction to which a bias voltage is applied. A diode allows current to flow primarily in the forward bias direction. In this case, the contact potential and therefore the electric field within the transition zone decreases. Hence, carriers which were generated inside the depletion zone I_0 can diffuse out and reach the source. The probability of diffusion increases with the Boltzmann factor $\exp[qV_f/kT]$. Since the contact potential lowers this electric field, the actual current is:

$$I = I_0 \left(\exp[qV/kT] - 1\right)$$

with

$$V = V_f - V_0$$

For significant current flow, a turn on voltage of $V_f = V_0$ is needed. This voltage allows the carriers to overcome the barrier.

When biased in the other direction, a smaller negative current (the dark current) $-I_0$ will flow. This is because of the reversed field in the transition zone. In the reverse direction, the height of the barrier doesn't effect this current, since the carriers don't cross the interface.

Further increasing of the reverse bias leads the valence band of the p-type region to approach the conduction band of the n-type region. When those bands are close enough, electrons can tunnel through the barrier and Zener breakdown occurs. This effect requires a highly doped material so that the width of the transition zone is sufficiently small. Zener breakdown is most dominant at low voltages ($\sim -5...-10V$). For lightly doped material, the breakdown occurs at higher voltages. Then the carriers of the dark current are so much accelerated by the reverse bias that they

ionize other atoms. This effect is called avalanche breakdown.

Resistivity The resistance of a diode can be calculated from the I-V curve. The current of a diode is not proportional to the applied voltage. Therefore it is called a differential resistance. To get an estimate of the resistance of a diode the almost linear part of the curve is taken. The resistance depends on the geometry and the conductivity σ of the material:

$$R = \frac{L}{wt}\frac{1}{\sigma} = R_s \frac{w}{L}\frac{1}{t\sigma}$$

with L=length, w=width, t=thickness and R_s =sheet resistance. We measured a sheet resistance of our wafer before doping $R_s = 87.6$ Ohm/Area, and after doping $R_s = 2.79$ Ohm/Area.

The conductivity depends on the dopant concentration n and the mobility μ of the carriers:

$$\sigma = qn\mu$$

with q=charge of the carriers.

With measurements of the sheet resistance, the dopant level can be calculated. If we assume the mobility for n-type carriers being $\mu_n \approx 600\mathrm{m}^2(\mathrm{sV})^{-1}$ and for p-type $\mu_p \approx 480\mathrm{m}^2(\mathrm{sV})^{-1}$, then at room temperature when $N_D \approx n_0$ respectively $N_A \approx p_0$:

$$N_D = (qtR_S\mu_n)^{-1} = 1.5 \times 10^17\mathrm{cm}^{-3} \quad (13)$$

$$N_A = (qtR_S\mu_p)^{-1} = 4.2 \times 10^15\mathrm{cm}^{-3} \quad (14)$$

C pn-Junctions

A pn-junction is the interface between a p-type region (doped with acceptors) and an n-type region (doped with donors). In equilibrium, the Fermi levels of these materials adjust. This means that electrons flow until the levels are equal. However, since p-type and n-type silicon even of same crystal and impurity concentration, have different Fermi levels with respect to their band edges, these bands must bend.

This adjustment takes place only in a limited region across the junction. This region is called the depletion zone, in which the carrier flow and the band bending occur. For a charge carrier to cross this region, it has to overcome a potential barrier, the so called contact potential V_0, which is equal to the shift of the bands due to the constancy of the Fermi level. This energy shift of the bands of the differently doped semiconductor leads to a lower conduction band of the n-type region. The Fermi-Dirac distribution gives the ratio of the carrier densities on both sides of the interface:

$$\frac{n_n}{n_p} = \exp[qV_0/kT] = \frac{N_C \exp[-(E_{Cn} - E_{Fn})/kT]}{N_C \exp[-(E_{Cp} - E_{Fp})/kT]}$$

where

$$E_{Fn} = E_{Fp}$$

then

$$qV_0 = E_{Cp} - E_{Cn}$$

Hence, for a given dopant level N_A and N_D, the contact potential can be calculated:

$$V_0 = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}$$

The width W of this depletion zone depends on the contact potential and the number of impurities, since a higher impurity concentration allows one to create the same

space charge in a much smaller volume. The relationship is:

$$W = \left[\frac{2\epsilon V_0}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) \right]^{1/2}$$

The penetration of the depletion zone into the n- and p-type material is:

$$x_{n0} = \frac{W}{1 + N_D/N_A}$$

respectively:

$$x_{p0} = \frac{W}{1 + N_A/N_D}$$

This biasing of pn-junctions leads to a raising and lowering of the electric field in the depletion zone. Since there is a neglectable resistance outside this region, the whole voltage appears just across the transition region. If the applied voltage is opposite to the contact potential, due to the migration of carriers, it is called forward bias. If the applied voltage increases the electric field across the transition zone, it is reverse bias.